

Description

Imaging Device and a Digital Camera Having Same

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional application of U.S. Patent Application Serial No. 09/441,233 filed November 16, 1999.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] This invention relates to imaging devices and, more particularly, to an imaging device which is applied, for example, for a digital camera having a plurality of pixel signals outputted through thinning out from a CCD imager.

[0003] This invention is also concerned with a digital camera having such an imaging device.

DESCRIPTION OF THE PRIOR ART

[0004] Referring to Figure 32, a conventional imaging device has had a CCD imager that is mounted, at its front, with a

complementary color filter having color components Ye, Cy, Mg and G so that pixel signals containing all kinds of complementary color components can be read from pixel blocks each having 2 pixels \times 8 lines. That is, G and Mg pixel signals are read from a first line of each pixel block, while Ye and Cy pixel signals are from a sixth line. The pixel signals thus read are then subjected to an interpolation process. As a result, thinned-out image signals are created wherein each pixel has all the color components.

[0005] In the prior art, however, there has been a problem that each pixel block requires twice horizontal transfers, consuming a considerable time in outputting pixel signals. This problem becomes more prominent as the number of pixel signals read from each pixel block is increased in order to improve resolution of the images having been thinned out.

SUMMARY OF THE INVENTION

[0006] It is therefore a primary object of the present invention to provide an imaging device which is reduced in time needed to output pixel signals.

[0007] Another object of the invention is to provide an imaging device which can output an increased number of pixel signals in a brief time.

[0008] A still another object of the invention is to provide a digital camera which is reduced in time needed to create an image.

[0009] A further object of the invention is to provide a digital camera which can create an image with increased resolution in a brief time.

[0010] An imaging apparatus according to the present invention, comprises: a color filter formed by a plurality of kinds of color elements; a CCD imager having pixels corresponding, in a one-to-one relation, to the color elements; and a timing generator for supplying a drive pulse to the CCD imager; wherein the color filter having color blocks formed by a plurality of rows each row having the plurality of kinds of color elements respectively assigned to the plurality of rows; the CCD imager having a plurality of rows of pixel blocks corresponding to the color blocks; the drive pulse including a read pulse to read from each of the plurality of rows pixel signals different in kind of said plurality of color elements, a vertical transfer pulse to cause vertical transfer of the pixel signals, and a horizontal transfer pulse to cause horizontal transfer of the pixel signals each time vertical transfer related to the number of vertical pixels of the pixel block has been completed.

[0011] In this invention, a color filter having a plurality of kinds of color elements is mounted on a light receiving surface of a CCD imager of an interline transfer scheme. The pixels of the CCD imager correspond, in a one-to-one relation, to color components of the color filter. The timing generator supplies a drive pulse to the CCD imager thus constructed. Here, the color filter has a plurality of rows of color blocks each row of which is assigned with the plurality of kinds of color elements at least one in number per kind. Also, the CCD imager has a plurality of rows of pixel blocks corresponding to the color blocks. If a read pulse is supplied to the CCD imager, pixel signals corresponding to different color elements are read from a plurality of rows forming the pixel block. The pixel signals read from the pixel block are vertically transferred by a vertical transfer pulse. Horizontal transfer is implemented according to a horizontal transfer pulse each time vertical transfer has been completed by the number of vertical pixels of the pixel block.

[0012] According to the invention, because the pixel signals read from the pixel block is horizontally transferred in a collective fashion, it is possible to reduce a time required for output as compared to the conventional, or to output

much more pixel signals in a same time as that of the conventional.

[0013] According to one embodiment, the read pulse is a pulse to read one pixel of the pixel signals from each row of the pixel blocks.

[0014] According to another embodiment, the color block includes different kinds of color elements on a same row. Also, the read pulse includes a first read pulse to read from the plurality of rows pixel signals corresponding to one part of the plurality of kinds of color elements and a second read pulse to read from the plurality of rows pixel signals corresponding to the remaining part of the plurality of kinds of color elements.

[0015] According to yet another embodiment of the invention, the color block includes two pixels or more of a same kind of a color element on a same row, and the read pulse is a pulse to read a plurality of pixels of pixel signals from each row of the pixel block.

[0016] According to still another embodiment of the invention, the CCD imager has a plurality of pixel blocks, and the read pulse is a pulse to read the pixel signals from each of the pixel blocks in such a manner as to give an even distance between lines including pixels to be read out.

[0017] According to another embodiment of the invention, the color filter has one part of the plurality of kinds of color elements on an odd-numbered line and another part of the plurality of kinds of color elements on an even-numbered line. Preferably, the plurality of kinds of color elements are an element G, an element Mg, an element Ye and an element Cy, the element G and the element Mg being arranged alternately every pixel on one of the odd numbered and even numbered lines, and the element Ye and the element Cy being arranged alternately every pixel on the other of the odd numbered and even numbered lines.

[0018] A digital camera according to the present invention, comprises: a color filter formed by a plurality of kinds of color elements; a CCD imager having pixels corresponding, in a one-to-one relation, to the color elements; a timing generator for supplying a drive pulse to the CCD imager; and an interpolation circuit for performing interpolation on a pixel signal outputted from the CCD imager; wherein the color filter having color blocks formed by a plurality of rows having the plurality of kinds of color elements respectively assigned to the plurality of rows; the CCD imager having a plurality of rows of pixel blocks corre-

sponding to the color blocks; the drive pulse including a read pulse to read from each of the plurality of rows pixel signals different in kind of the plurality of color elements, a vertical transfer pulse to cause vertical transfer of the pixel signals, and a horizontal transfer pulse to cause horizontal transfer of the pixel signals each time vertical transfer related to the number of vertical pixels of the pixel blocks has been completed.

[0019] In this invention, a color filter having a plurality of kinds of color elements is mounted on a light receiving surface of a CCD imager of an interline transfer scheme. The pixels of the CCD imager correspond, in a one-to-one relation, to color components of the color filter. The timing generator supplies a drive pulse to the CCD imager thus constructed. Responsive to the drive pulse, the pixel signals outputted from the CCD imager is interpolated by an interpolation circuit. Here, the color filter has a plurality of rows of color blocks each row of which is assigned with the plurality of kinds of color elements at least one in number per kind. Also, the CCD imager has a plurality of rows of pixel blocks corresponding to the color blocks. If a read pulse is supplied to the CCD imager, pixel signals corresponding to different color elements are read from a

plurality of rows forming the pixel block. The pixel signals read from the pixel block are vertically transferred by a vertical transfer pulse. Horizontal transfer is implemented according to a horizontal transfer pulse each time vertical transfer has been completed by the number of vertical pixels of the pixel block.

[0020] According to one embodiment, an image corresponding to an output of the interpolation circuit is displayed on a monitor.

[0021] According to this invention, because the pixel signals read from the pixel block are horizontally transferred in a collective fashion, it is possible to reduce a time required to create one scene of thinned-out image as compared to the conventional, or to create a thinned-out image with improved resolution in a same time as that of the conventional.

[0022] The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Figure 1 is a block diagram showing an embodiment of

the present invention;

[0024] Figure 2 is an illustrative view showing one example of a complementary color filter;

[0025] Figure 3 is an illustrative view showing another example of a complementary color filter;

[0026] Figure 4(A) is an illustrative view showing one part of a CCD imager;

[0027] Figure 4(B) is a timing chart showing operation of drive pulses;

[0028] Figure 5 is an illustrative view showing operation of the CCD imager;

[0029] Figure 6(A) is an illustrative view showing one part of the CCD imager shown in Figure 5;

[0030] Figure 6 is an illustrative view showing another part of the CCD imager shown in Figure 5;

[0031] Figure 7(A) is a timing chart showing operation of drive pulses;

[0032] Figure 7(B) is an illustrative view showing a state of charge transfer;

[0033] Figure 7(C) is an illustrative view showing a state of charge transfer;

[0034] Figure 8 is an illustrative view showing operation of another CCD imager;

- [0035] Figure 9(A) is an illustrative view showing one part of the CCD imager shown in Figure 8;
- [0036] Figure 9(B) is a illustrative view showing another part of the CCD imager shown in Figure 8;
- [0037] Figure 10(A) is a timing chart showing operation of drive pulses;
- [0038] Figure 10(B) is an illustrative view showing a state of charge transfer;
- [0039] Figure 10(C) is an illustrative view showing a state of charge transfer;
- [0040] Figure 11 is an illustrative view showing operation of another CCD imager;
- [0041] Figure 12(A) is an illustrative view showing one part of the CCD imager shown in Figure 11;
- [0042] Figure 12(B) is an illustrative view showing another part of the CCD imager shown in Figure 11;
- [0043] Figure 13 is a timing chart showing operation of drive pulses;
- [0044] Figure 13(B) is an illustrative view showing a state of charge transfer;
- [0045] Figure 13(C) is an illustrative view showing a state of charge transfer;
- [0046] Figure 14 is an illustrative view showing operation of an–

other CCD imager;

[0047] Figure 15(A) is an illustrative view showing one part of the CCD imager shown in Figure 14;

[0048] Figure 15(B) is an illustrative view showing another part of the CCD imager shown in Figure 14;

[0049] Figure 16(A) is a timing chart showing operation of drive pulses;

[0050] Figure 16(B) is an illustrative view showing a state of charge transfer;

[0051] Figure 16(C) is an illustrative view showing a state of charge transfer;

[0052] Figure 17 is an illustrative view showing operation of another CCD imager;

[0053] Figure 18(A) is an illustrative view showing one part of the CCD imager shown in Figure 17;

[0054] Figure 18(B) is an illustrative view showing another part of the CCD imager shown in Figure 17;

[0055] Figure 19(A) is a timing chart showing operation of drive pulses;

[0056] Figure 19(B) is an illustrative view showing a state of charge transfer;

[0057] Figure 19(C) is an illustrative view showing a state of charge transfer;

- [0058] Figure 20 is an illustrative view showing operation of another CCD imager;
- [0059] Figure 21(A) is an illustrative view showing one part of the CCD imager shown in Figure 20;
- [0060] Figure 21(B) is an illustrative view showing another part of the CCD imager shown in Figure 20;
- [0061] Figure 22(A) is a timing chart showing operation of drive pulses;
- [0062] Figure 22(B) is an illustrative view showing a state of charge transfer;
- [0063] Figure 22(C) is an illustrative view showing a state of charge transfer;
- [0064] Figure 23 is an illustrative view showing operation of another CCD imager;
- [0065] Figure 24(A) is an illustrative view showing one part of the CCD imager shown in Figure 23;
- [0066] Figure 24(B) is an illustrative view showing another part of the CCD imager shown in Figure 23;
- [0067] Figure 25(A) is a timing chart showing operation of drive pulses;
- [0068] Figure 25(B) is an illustrative view showing a state of charge transfer;
- [0069] Figure 25(C) is an illustrative view showing a state of

charge transfer;

[0070] Figure 26 is an illustrative view showing operation of still another CCD imager;

[0071] Figure 27(A) is an illustrative view showing one part of the CCD imager shown in Figure 26;

[0072] Figure 27(B) is an illustrative view showing another part of the CCD imager shown in Figure 26;

[0073] Figure 28(A) is a timing chart showing operation of drive pulses;

[0074] Figure 28(B) is an illustrative view showing a state of charge transfer;

[0075] Figure 28(C) is an illustrative view showing state of charge transfer;

[0076] Figure 29 is an illustrative view showing operation of another CCD imager;

[0077] Figure 30(A) is an illustrative view showing one part of the CCD imager shown in Figure 29;

[0078] Figure 30(B) is an illustrative view showing another part of the CCD imager shown in Figure 29;

[0079] Figure 31(A) is a timing chart showing operation of drive pulses;

[0080] Figure 31(B) is an illustrative view showing a state of charge transfer;

[0081] Figure 31(C) is an illustrative view showing a state of charge transfer; and

[0082] Figure 32 is an illustrative view showing operation of a conventional CCD imager.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0083] Referring to Figure 1, a digital camera 10 of this embodiment includes an optical lens 12. An optical image of a subject given through the optical lens 12 is taken in a vertically-inverted position to a CCD imager 16 that is of an interline transfer scheme provided inside an imaging apparatus 14. The CCD imager 16 is mounted, on its light receiving surface, with a complementary color filter 16a shown in Figure 2 so that each light receiving element (sensor) can create a pixel signal having any of color components Ye, Cy, Mg and G.

[0084] In a camera mode to display real-time motion images (through-images) on a monitor 36, a timing generator (TG) 18 reads out pixel signals due to thinning out. As a consequence, only the pixel signals created on particular light receiving elements are read out of the CCD imager 16 and supplied to a CDS/AGC circuit 24. The pixel signals are subjected to well-known noise removal and level adjustment by the CDS/AGC circuit 24, and the pixel sig-

nals thus processed are converted by an A/D converter 26 into pixel data as a digital signal.

[0085] The pixel data is stored into a memory 30 through a digital clamp circuit 28, and thereafter read therefrom. The read pixel data is inputted directly or through line memories 32a – 32c to a signal processing circuit 34a. The signal processing circuit 34a performs interpolation on the pixel data and creates pixel data that each pixel contain all the 4 color components. The signal processing circuit 34 also performs RGB conversion and YUV conversion on the interpolated pixel data, and outputs the obtained YUV data to the monitor 36. As a result, through-images are displayed on the monitor 36.

[0086] Incidentally, if an operator depresses a shutter button (not shown), the TG18 performs so-called all pixel read out. As a result, a still image is obtained that is improved in resolution over that in the camera mode.

[0087] Referring to Figure 2, the complementary color filter 16a includes color components Ye, Cy, Mg and G. These color components correspond to the pixels of the CCD imager 16, so that each light receiving element of the CCD imager 16 can create a pixel signal having any one color component. Observing the complementary color filter 16a of

Figure 2 along a horizontal direction, G and Mg are alternately arranged every other pixel on an odd-numbered line, while Ye and Cy are alternately arranged every other pixel on an even-numbered line. Meanwhile, looking the complementary color filter 16a in a vertical direction, G and Ye are alternately arranged every other pixel on an odd-numbered vertical row, while Mg and Cy are alternately arranged every other pixel on an even-numbered vertical row. This means that the complementary color filter 16a includes a plurality of matrixes each having vertically 2 pixels and horizontally 2 pixels (2×2 matrix). The complementary color filter 16a thus structured is mounted on the CCD imager 16.

[0088] Referring to Figure 5, it is considered in this embodiment that the complementary color filter 16a is a gathering of color blocks CB1 each having 8 lines \times 4 rows while the CCD imager 16 a gathering of corresponding pixel blocks CB1 to the color blocks CB1. Each block is assigned, on each row, with all the color components of at least one in number per color. A common process is applied to these blocks. Specifically, in each block, pixel signals at line 1 are read from rows 1 and 2, and pixel signals at line 6 are read from rows 3 and 4. Each read pixel signal possesses

color components G, Mg, Ye and Cy. These pixel signals are vertically transferred, and then horizontally transferred in a collective fashion at a time that 4 pixel signals have been collected on a horizontal transfer register. As a result, the G, Mg, Ye and Cy pixel signals obtained from a same block are outputted from the CCD imager 16 due to once horizontal transfer.

[0089] As shown in Figure 6(A) and Figure 6(B), each light receiving element is assigned with two vertical transfer registers. Each vertical transfer register is given any one of drive pulses V1a, V1b, V2 and V3a, V3b and V4. These drive pulses are all created by a V driver 20 based on a vertical transfer pulse and charge read pulse outputted from the TG18.

[0090] As can be understood from Figure 6(A), for the G/Mg pixels on rows 1 and 2, a drive pulse V1a or V1b is applied to one vertical transfer register while a drive pulse V2 is to the other vertical transfer register. In this embodiment, because for rows 1 and 2 the G and Mg pixels on line 1 are to be thinned out, the drive pulse V1b is supplied only to the pixels on line 1. For the Ye/Cy pixels on rows 1 and 2, a drive pulse V is applied to one vertical transfer register while a drive pulse V4 is to the other vertical transfer

register. Note that there is no case of using a drive pulse V3b for rows 1 and 2.

[0091] Referring to Figure 6(B), on rows 3 and 4, other drive pulses than the drive pulse V1b are applied to a predetermined vertical transfer register. That is, a drive pulse V1a is applied to a vertical transfer register for one of the G/Mg pixels, while a pulse V2 is to the other vertical transfer register. Also, a drive pulse V3a or V3b is applied to a vertical transfer register for one of Ye, Cy pixels, while a drive pulse V4 is to the other vertical transfer register. In this embodiment, because the Ye/Cy pixels on line 6 of rows 3 and 4 are to be read out, the drive pulse V3b is supplied only to the pixel on line 6.

[0092] In order to allow for all-the-pixels reading and thinning out, two drive pulses V1a and V1b are assigned to one of the vertical transfer registers for the G/Mg pixels on rows 1 and, while two drive pulses V3a and V3b are one of the vertical transfer registers for the Ye/Cy pixels on rows 3 and 4. The drive pulses V1b and V3b are assigned respectively to the G/Mg pixels and Ye/Cy pixels to be thinned out and read out. This is true for other embodiment in respect of assigning the drive pulses V1a and V1b and the drive pulses V3a and V3b in a manner as stated above.

[0093] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 7(A). In a period

①

, the drive pulses V3a and V3b assume a zero level and the remaining drive pulses all assume a minus level. In a duration

②

, the drive pulse V3b changes to a plus level and the drive pulse V4 changes to the zero level. As a result, in each block, pixel signals are read from line 6 on rows 3 and 4, as shown in Figure 7(C). That is, charges are read onto one of the vertical transfer registers on line 6 so that the read charges are stored on the two vertical transfer registers on the line 6. In a period

③

, the drive pulses V1a, V1b and V3b change to the zero level. Due to this, charge reading is suspended and the charges read from line 6 is also stored onto a corresponding one of the vertical transfer registers to line 5.

[0094] The drive pulse V1b in a period

④

becomes a plus level with a result that, as shown in Figure 7(B), pixel signals are read from line 1 on rows 1 and 2. That is, charges are read onto corresponding one vertical transfer register to the line 1. At this time, because the drive pulses V3a and V4a are zero in level, the read charges are also stored to corresponding two vertical transfer registers to the line 2. When a period

⑤

is reached, the drive pulse V1b becomes a zero level thus suspending the charge reading. The pixel signals read from line 1 on the rows 1 and 2 as well as the line 6 on the rows 3 and 4 are vertically transferred in a separate fashion in or after the period

⑤

. Incidentally, the drive pulses V1b and V3b become a plus level when the charge read pulse outputted from the TG18 becomes a high level.

[0095] Each time vertical transfer is completed by a corresponding distance to the number of vertical pixels within the block, drive pulses H1 and H2 shown in Figure 4(B) are outputted from an H driver 22. The drive pulses H1 and H2 are reverse in polarity to each other, i.e. when one is in

a high level the other assumes a low level. As shown in Figure 4(A) the drive pulse H1 is applied to a horizontal transfer register provided at the ends of the vertical transfer registers. Meanwhile, the drive pulse H2 is supplied to a horizontal transfer register provided at the ends of the sensors. The vertical pulses H1 and H2 start changing in level at a time that vertical transfer by one block has completed. This causes pixel signals to be transferred in a horizontal direction. That is, the pixel signals created in the blocks are horizontally transferred in a collective fashion.

[0096] The signal processing circuit 34a performs interpolation on the corresponding pixel data to the pixel signals thus outputted. As a result, thinned-out image data is created that each pixel has all the color components.

[0097] In this embodiment, each clock requires only once horizontal transfer, thus reducing a time needed to read pixel signals as compared to that of the conventional. This means that assuming the number of pixels on the CCD imager 16 is the same as the conventional, the read time is reduced to a half of that of the conventional.

[0098] Figure 8 to Figure 10 shows a modification to the CCD imager 16 of Figure 1. In also this embodiment, the CCD

imager 16 is mounted with a complementary color filter 16a. It is considered that this complementary filter 16a is a gathering of color blocks CD1 each having 8 lines \times 4 rows. Hence, the CCD imager 16 is also considered as a gathering of corresponding pixel blocks PB1 to the color blocks CB1. In this embodiment, however, in each block at lines 1 and 5 pixel signals are read from rows 1 and 2 while at lines 2 and 6 pixel signals are read from rows 3 and 4. In other words, two pixel signals per G, Mg, Ye and Cy are read from each block. The read pixel signals are vertically transferred in a separate fashion and accumulated on the horizontal transfer register. Horizontal transfer is performed once each time vertical transfers by 8 lines has been completed. Due to this, the pixel signals having a same color component are mixed with each other over the horizontal transfer register. Although the color component of the pixel signal to be outputted by once horizontal transfer changes in the order of G, Mg, Ye and Cy similarly to the Figure 1 embodiment, the pixel signals have a nearly twice level as compared to those of the Figure 1 embodiment.

[0099] Referring to Figure 9(A) and Figure 9(B), in also this embodiment each light emitting element is assigned with two

vertical transfer registers, wherein each vertical transfer register is applied by one of drive pulses V1a, V1b, V2, V3a, V3b and V4.

[0100] However, at rows 1 and 2 there is a need to read pixel signals from lines 1 and 5. Accordingly, as will be understood from Figure 9(A), a drive pulse V1a is applied to the G/Mg pixels on lines 3 and 7 while a drive pulse V1b is to the G/Mg pixels on lines 1 and 5. Also, at rows 3 and 4 there is a need to read pixel signals from lines 2 and 6. Accordingly, as shown in Figure 9(B) a drive pulse V3a is supplied to lines 4 and 8 while a drive pulse V3b is to lines 2 and 6.

[0101] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 10(A). These changes are quite the same as those of Figure 7(A). However, unlike the Figure 1 embodiment, the drive pulse V1b is supplied also to line 5 on rows 1 and 2 while the drive pulse 3b is given also to line 2 on rows 3 and 4. Due to this, as shown in Figure 10(B) and Figure 10(C), charges are read also from line 5 on row 1 and 2 as well as from line 2 on the rows 3 and 4. The charges are vertically transferred in a separate fashion in and after a period

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[0102] Each time a pixel signal read from each block is accumulated onto the horizontal transfer register, drive pulses H1 and H2 shown in Figure 4(B) are supplied to the horizontal transfer register. The pixel signal is transferred in a horizontal direction in response to the drive pulses H1 and H2. That is, 8 pixels of pixel signals created by each block are horizontally transferred in a collective manner. A signal processing circuit 34a performs interpolation similarly to the Figure 1 embodiment. As a result, image data is created that has all the color components for each pixel.

[0103] According to this embodiment, the number of times of horizontal transfers for each block can be reduced to once and further the pixel signal is increased in level twice that of the conventional.

[0104] Figure 11 to Figure 13 show another modification of a CCD imager 16. This CCD imager 16 is also amounted with a complementary color filter 16a. It however is considered that the complementary color filter 16a is a gathering of color blocks CB2 each having 4 lines \times 4 rows and the CCD imager 16 is a gathering of corresponding pixel blocks PB2 to the color blocks CB2. Every block is applied by a common process. That is, in each block, at

line 1 pixel signals are read from rows 1 and 2, and at line 2 pixel signals are read from rows 3 and 4. The read pixel signals each has color components G, Mg, Ye and Cy. The pixel signals are vertically transferred. When 4 pixel signals have been collected onto a horizontal transfer register, i.e. when vertical transfer by 4 lines has been completed, these pixel signals are horizontally transferred in a collective fashion. As a result, the color components G, Mg, Ye and Cy are repeatedly included in the pixel signals outputted by once horizontal transfer.

[0105] As shown in Figure 12(A), on rows 1 and 2, a drive pulse V1b is applied to the G/Mg pixels on line 1 while a drive pulse V1a is to the G/Mg pixels on line 3. Also, as shown in Figure 12(B) on rows 3 and 4, a drive pulse V3b is supplied to the Ye/Cy pixels on line 2 while a drive pulse V3a is to the Ye/Cy pixels on line 4.

[0106] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 13(A). These changes are quite the same as those of Figure 10(A). This embodiment and the embodiment of Figure 8 to Figure 10 are different in conception about the block but same in the pixels to be read out. Accordingly, the timings of charge read out and transfer shown in Figure 13(B) and Figure 13(C) are same as those

of Figure 10(B) and Figure 10(C).

[0107] Because of the difference in conception about the block, horizontal transfer is conducted in different timing from that of the Figure 8 to Figure 10 embodiment. That is, in the Figure 8 embodiment horizontal transfer is done each time pixel signals by 8 lines have been vertically transferred whereas in this embodiment horizontal transfer is conducted each time vertical transfer by 4 lines has been completed.

[0108] In the signal processing circuit 34a, interpolation is performed similarly to the above. As a result, image data is created that each pixel has all the color components.

[0109] According to this embodiment, there is increase in pixel signal reading time by the increase in the number of times of horizontal transfers. It however is possible to increase twice the vertical resolution of the thinned-out image signal as compared to that of the conventional.

[0110] Figure 14 to Figure 16 show a still another modification of a CCD imager 16. The CCD imager 16 is mounted with a complementary color filter 16a, similarly to the above. It can be considered that the complementary color filter 16a is a gathering of color block CB2 each having 4 lines × rows while the CCD imager 16 is a gathering of corre-

sponding pixel blocks PB2 to the color blocks CB2. Every block is applied by a common process. However, in each block, on lines 1 and 3 pixel signals are read from rows 1 and 2, while on lines 2 and 4 pixel signals are read from lines 3 and 4. The read pixel signals each have color components G, Mg, Ye and Cy. The pixel signals are vertically transferred. When vertical transfer by 4 lines has been completed, the pixel signals are horizontally transferred in a collective fashion. Due to this, the pixel signals having a same color component are mixed with each other over a horizontal transfer register and then outputted from the CCD imager 16. Each pixel signal has a level twice that of the Figure 11 to Figure 13 embodiment.

[0111] In each block, on rows 1 and 2 a drive pulse V1b is applied to all the G/Mg pixels without using a drive pulse V1a, as shown in Fig. 15(A). On rows 3 and 4, on the other hand, a drive pulse V3b is applied to all the Ye, Cy pixels without using a drive pulse V3a, as shown in Figure 13(B).

[0112] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 16(A), similarly to those of Figure 13(A). However, because a drive pulse V1b is applied to all the G/Mg pixels on rows 1 and 2, charges are read from both lines 1 and 3. Also, because the drive pulse V3b is applied

to all the Ye/Cy pixels on rows 3 and 4, charges are read from both lines 2 and 4, as shown in Figure 16(C).

[0113] The read charges are vertically transferred in a separate manner, and thereafter horizontally transferred in timing of once every 4 lines responsive to drive pulses H1 and H2. This means that the pixel signals possessing a same color component are mixed with each other over the horizontal transfer register, hence outputting mixed pixel signals. The output pixel signals vary in color component in the order of G, Mg, Ye and Cy, similarly to the above embodiment. The pixel data corresponding to the output pixel signals is interpolated by a signal processing circuit 34a. As a result, thinned-out image data is created that has each pixel has all the color components.

[0114] According to this embodiment, there is increase in time to read out a pixel signal because of increase in the number of times of horizontal transfers. It is however possible to improve twice the pixel signal level and thinned-out image data vertical resolution as compared to those of the conventional. Also, a returning characteristic is obtained constant because of an even distance between the line that G and Mg pixel signals are to be read out and the line that Ye and Cy pixel signals are to be read out. Thus, fil-

tering is facilitated.

[0115] Referring to Figure 17 to Figure 19, a CCD imager 16 of another modification is mounted with a complementary color filter 16b of Figure 3. The complementary color filter 16b includes color components Ye, Cy, Mg and G similarly to the complementary color filter 16a. These color components correspond to pixels on the CCD imager 16. When observing the complementary color filter 16b along a horizontal direction, on an odd-numbered line are alternately arranged G and Mg every other pixel while on an even-numbered line are alternately arranged Ye and Cy every other pixel, similarly to the complementary color filter 16a. However, Mg and G are inverted in position on every odd-numbered line. Where the color component on an odd-numbered line being considered varies as Mg, G, Mg, G ..., the color components on a preceding and succeeding odd-numbered lines vary as G, Mg, G, Mg Consequently, when observing the complementary color filter 16b along a vertical direction, the color components are arranged in the order of G, Ye, Mg and Ye on an odd-numbered row, while on an even-numbered row the color components are arranged in the order of Mg, Cy, G and Cy. This means that the complementary color filter 16b is

formed with a plurality of matrixes (2×4 matrix) each having vertically 2 pixels and horizontally 4 pixels. The complementary color filter 16b thus configured is mounted on the CCD imager 16.

[0116] Referring to Figure 17, it is considered in this embodiment that the complementary color filter 16b is a gathering of color blocks CB1 each having 8 lines \times 4 rows while CCD imager 16 is a gathering of corresponding pixel blocks PB1 to the color blocks CB1. In each block, on line 1 pixel signals are read from rows 1 and 2 while on line 6 pixel signals are read from rows 3 and 4. That is, pixel signals of one in number per G, Mg, Ye and Cy are read out of each block. The read pixel signals are vertically transferred in a separate fashion, and accumulated onto a horizontal transfer register. The horizontal transfer is carried out each time vertical transfer by 1 line has been completed. As a result, the pixel signals outputted in one horizontal transfer vary in color component in the order of G, Mg, Ye and Cy.

[0117] As shown in Figure 18(A), on rows 1 and 2 a drive pulse V1b is applied only to the G/Mg pixels on line 1. Also, on rows 3 and 4 a drive pulse V3b is supplied only to the Ye/Cy pixels on line 6, as shown in Figure 18(B).

[0118] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 19(A), similarly to those of other embodiments. Because the drive pulse V1b is supplied only to line 1 on rows of 1 and 2, charges are read out of these rows as shown in Figure 19(B). Also, because a drive pulse V3b is supplied only to the line 6 on the rows 3 and 4, charges are read out of these rows as shown in Figure 19(C). The read charges are vertically transferred in a separate fashion.

[0119] Each time the pixel signals read out of each block are accumulated onto a horizontal transfer register, i.e. each time vertical transfer by 8 lines has been completed, drive pulses H1 and H2 shown in Figure 4(B) are applied to the horizontal transfer register. Responsive to these drive pulses H1 and H2, the pixel signals are transferred in a horizontal direction. This means that 4 pixels of pixel signals created in each block are horizontally transferred in a collective fashion. The signal processing circuit 34a performs similar interpolation to that Figure 1 embodiment. As a result, thinned-out image data is created that each pixel has all the color components.

[0120] According to this embodiment, because each block requires only once horizontal transfer, it is possible to re-

duce a time required to read out pixel signals as compared to the conventional.

[0121] Figure 20 to Figure 22 show another modification of a CCD imager 16, which is also mounted with a complementary color filter 16b. It is considered in this embodiment that the complementary color filter 16b is a gathering of color blocks CB2 each having 4 lines \times 4 rows while the CCD imager 16 is a gathering of pixel blocks PB2 corresponding to the color blocks CB2. In each block, on line 1 pixel signals are read from rows 1 and 2 while on line 2 pixel signals are read from rows 3 and 4. The read pixel signals each have color components G, Mg, Ye and Cy. The pixel signals thus configured are transferred in a vertical direction. At a time that 4 pixel signals are collected on a horizontal transfer register, i.e. when vertical transfer by 4 lines has been completed, the pixel signals are horizontally transferred in a collective fashion. As a result, the pixel signals outputted in once horizontal transfer repeatedly contain color components G, Mg, Ye and Cy.

[0122] As shown in Figure 21(A), on rows 1 and 2 a drive pulse V1b is applied to the G/Mg pixels on line 1 while a drive pulse V1a is to the Mg/G pixels on line 3. Also, as shown in Figure 21(B), on rows 3 and 4 a drive pulse V3b is sup-

plied to the Ye/Cy pixels on line 2 while a drive pulse V3a is to the Ye/Cy pixels on line 4.

[0123] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 22(A), similarly to those in the other embodiments. With such drive pulses, on rows 1 and 2 charges are read only from line 1 as shown in Figure 22(B) while on rows 3 and 4 charges are read only from line 2 as shown in Figure 22(C). The read charges are vertically transferred in a separate fashion, and delivered to a horizontal transfer register. Horizontal transfer is carried out each time vertical transfer by 4 lines has been completed. As a result, 4 pixels of pixel signals read out of a same block are collectively outputted. The output pixel signals are subjected to interpolation by the signal processing circuit 34. Thus, thinned-out image data is created that each pixel has all the color components.

[0124] According to this embodiment, there is increase in time to read pixel signals because of increase in the number of times of horizontal transfers. It is however possible to improve twice thinned-out image signal vertical resolution as compared to the conventional.

[0125] Figure 23 to Figure 25 show another modification of a CCD imager 16, which is also mounted with a comple-

mentary color filter 16b. It is considered that the complementary color filter 16b is a gathering of color blocks CB2 each having 4 lines \times 4 rows while the CCD imager 16 is a gathering of corresponding pixel blocks PB2 to the color blocks CB2. In each block, on lines 1 and 2 pixel signals are read from rows 1 and 2 while on lines 3 and 4 pixel signals are read from rows 3 and 4. On row 1, G and Ye pixel signals are obtained wherein both the pixel signals are mixed with each other during reading out. On row 2, Mg and Cy pixel signals are read out wherein these pixel signals are mixed with each other during reading out. Similarly, on the row 3 Mg and Ye pixel signals are obtained, and on row 4 G and Cy pixel signals are obtained. Then, the pixel signals on a same row are mixed with each other. The pixel signals thus mixed are delivered to the horizontal transfer register. When vertical transfer by 4 lines has been completed, these pixel signals are horizontally transferred in a collective fashion. The pixel signals outputted in once horizontal transfer include repetitively color components (G + Ye), (Mg + Cy), (Mg + Ye) and (G + Cy).

[0126] As shown in Figure 24(A), on rows 1 and 2 a drive pulse V1b is applied to the G/Mg pixels on line 1 while a drive

pulse 3b is to the Ye/Cy pixels on line 2. Also, as shown in Figure 24(B) on rows 3 and 4 a drive pulse V1b is supplied to the Mg/G pixels on line 3 while a drive pulse V3b is to the Ye/Cy pixels on line 4.

[0127] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 25(A), similarly to those of the other embodiments. On rows 1 and 2, as shown in Figure 25(B), charges are read from the line 2 in a period

②

and charges are read from the line 1 in a period

⑤

. Also, on the rows 3 and 4, as shown in Figure 25(C), charges are read from the line 4 in a period

②

and charges are read from the line 3 in a period

⑤

. In a period

④

the drive pulses V1b, V3b and V4 becomes a zero level, and in a period

⑤

the drive pulse V1b changes from the zero level to a plus level. This causes mixing of charges on each row. The mixed charges are thereafter vertically transferred. Each time vertical transfer by 4 lines has been completed, the charges are horizontally transferred.

[0128] Differently from the other embodiments, the pixel signals outputted from the CCD imager 16 have different color components having been mixed. These pixel signals are interpolated by the signal processing circuit 34b with a result that thinned-out image data is created that each pixel has all the color components. The signal processing circuit 34b creates YUV data as follows. Y data is determined by equation 1, U data is by equation 2, and V data is by equation 3.

[0129] [Equation 1]

$$\begin{aligned} Y &= \{(G + Ye) + (Mg + Cy) + (Mg + Ye) + (G + Cy)\} / 4 \\ &= \{(G + G + G) + (R + B + B + G) + (R + B + R + G) + (G + B + G)\} / 4 \\ &= (4R + 6G + 4B) / 4 \end{aligned}$$

[0130]

[Equation 2]

$$\begin{aligned}U &= \{(Mg + Ye) - (G + Cy)\} \\&= \{(R + B + R + G) - (G + B + G)\} \\&= 2R - G\end{aligned}$$

[0131]

[Equation 3]

$$\begin{aligned}V &= \{(G + Ye) - (Mg - Cy)\} \\&= \{(G + G + R) - (R + B + B + G)\} \\&= G - 2B\end{aligned}$$

[0132] According to this embodiment, there is increase in time to read out pixel signals due to increase in the number of times of horizontal transfers. It is however possible to improve twice the vertical resolution of a thinned-out image signal. Incidentally, although this embodiment was explained using the complementary color filter 16b with 2×4 matrixes, the pixel to be read out is in a 2×2 matrix

form and, accordingly, the complementary color filter 16a may be used in place of the complementary color filter 16b. Also, although in this embodiment pixel mixing was carried out over the vertical transfer register, pixel mixing may be conducted on the horizontal transfer registers.

[0133] Referring to Figure 26 to Figure 28, another modification of a CCD imager 16 is mounted with a complementary color filter 16a of Figure 2. It is considered in this embodiment that the complementary color filter 16a is a gathering of color blocks CB3 each having 12 lines \times 4 rows while the CCD imager 16 is a gathering of corresponding pixel blocks PB3 to the color blocks CB3. In each block, on line 1 pixel signals are read from rows 1 and 2, and on line 8 pixel signals are read from rows 3 and 4. As a result, each read pixel signal has color components G, Mg, Ye and Cy. The pixel signals thus configured are vertically transferred. When vertical transfer by 12 lines has been completed, the pixel signals are horizontally transferred in a collective fashion. The pixel signals outputted in once horizontal transfer contain color components G, Mg, Ye and Cy in this order.

[0134] For rows 1 and 2 in each block, a drive pulse V1b is applied to the G/Mg pixels on the line 1, as shown in Figure

27(A). Meanwhile, on the rows 3 and 4 a drive pulse V3b is supplied to the Ye/Cy pixels on line 8.

[0135] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 34(A), similarly to those of the other embodiments. Due to the drive pulse V1b applied to the G/Mg pixels on line 1 of rows 1 and 2, charges are read from line 1, as shown in Figure 28(B). Also, due to the drive pulse V3b applied to the Ye/Cy pixels on the line 8 of rows 3 and 4, charges are read from line 8, as shown in Figure 28(C).

[0136] The read charges are vertically transferred in a separate fashion, and then horizontally transferred in timing of once every 12 line according to the drive pulses H1 and H2. As a result, the pixel signals having G, Mg, Ye and Cy read out from each block are collectively outputted. The pixel data corresponding to the output pixel signals is interpolated by the signal processing circuit 34a. As a result, thinned-out image data is created that each pixel has all the color components.

[0137] According to this embodiment, each block requires only once horizontal transfer process and furthermore each block is constituted by an increased number of vertical pixels. It is therefore possible to greatly reduce a time re-

quired to read out pixel signals.

[0138] Referring to Figure 29 to Figure 31, another modification of a CCD imager 16 is mounted with a complementary color filter 16a of Figure 2. It is considered in this embodiment that the complementary color filter 16a is a gathering of color blocks CB4 each having 6 lines \times 4 rows while the CCD imager 16 is a gathering of corresponding pixel blocks PB4 to the color blocks CB4. In each block, on line 1 pixel signals are read out from rows 1 and 2, and on line 4 pixel signals are read from rows 3 and 4. As a result, the read pixel signals each possess color components G, Mg, Ye and Cy. These pixel signals are vertically transferred. At a time that vertical transfer by 6 lines has been completed, the pixel signals are horizontally transferred in a collective fashion. Similarly to the embodiment of Figure 26 to Figure 28, the pixel signals outputted in one horizontal transfer contain color components G, Mg, Ye and Cy in this order.

[0139] For rows 1 and 2 in each block, a drive pulse V1b is applied to the G, Mg pixels on line 1, as shown in Figure 30(A). On the other hand, for rows 3 and 4 a drive pulse V3b is supplied to the Ye/Cy pixels on line 4, as shown in Figure 30(B).

[0140] The drive pulses V1a, V1b, V2, V3a, V3b and V4 vary as shown in Figure 31(A), similarly to those of the other embodiments. Due to the drive pulse V1b applied to the G/Mg pixels on the line 1 of the rows 1 and 2, charges are read from the line 1 as shown in Figure 31(B). Also, due to the drive pulse V3b applied to the Ye/Cy pixels on line 4 of the rows 3 and 4, charges are read from line 4, as shown in Figure 31(C).

[0141] The read charges are vertically transferred in a separate fashion, and then vertically transferred in timing of once every 6 line. As a result, the pixel signals having G, Mg, Ye and Cy corresponding to the blocks are collectively outputted. The pixel data corresponding to the output pixel signals is interpolated by the signal processing circuit 34a similarly to the embodiment of Figure 26 to Figure 28. As a result, thinned-out image data is created that each pixel has all the color components.

[0142] According to this embodiment, each block requires only once horizontal transfer. It is therefore possible to reduce a time required to read out pixel signals. Also, a returning characteristic is given constant because of an even spacing between the line that G and Mg pixel signals are to be read and the line that Ye and Cy pixel signals are to be

read. Thus filtering is facilitated.

[0143] Incidentally, although this embodiment used the complementary color filter 16a, the use of a complementary color filter 16b will realize the similar function. Also, although in this embodiment the number of pixel signals to be read out of each row included in each block is determined one, a plurality of pixel signals may be read from each row provided that a distance between the lines from which the pixel signals are to be read. That is, it may be considered, without changing the pixels to be read out, that the complementary color filter 16a is a gathering of color blocks CB3 each having 12 lines \times 4 rows while the CCD imager 16 is a gathering of corresponding pixel blocks PB3 to the color blocks CB3.

[0144] Furthermore, in the above nine embodiments, reading with thinning-out is implemented only in the camera mode. It is however needless to say that this invention is applicable also for a case of recording thinned-out image data.

[0145] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the

present invention being limited only by the terms of the appended claims.